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E. Willis
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Atsuko KOZAI		
Appln. No.:	09/604,530	**Art Unit:**	2768
Filed:	June 27, 2000	**Examiner:**	To be assigned
For:	**STANDARD CELL, STANDARD CELL ARRAY, AND SYSTEM AND METHOD FOR PLACING AND ROUTING STANDARD CELLS**	**Docket No.:**	KOM-02001

Certificate of Mailing

I hereby certify that the foregoing documents are being deposited with the United States Postal Service as first class mail, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date of June 24, 2003.

Tracey Newell
Name: Tracey Newell

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO-1449 is a listing of documents known to Applicants and/or their attorney in compliance with the requirements of 37 CFR 1.56. Copies of the documents are also being submitted.

The references submitted herewith were cited by the Korean Patent Office in a May 30, 2003 Office Action (copy enclosed) for a counterpart application. Thus, since this Information Disclosure Statement is being filed within three months of that date and prior to a Final Office Action or Notice of Allowance, no fee is due.

In compliance with the requirements of 37 C.F.R. §1.98(a)(3), as a concise statement of relevance, as it is presently understood by the individual designated in 35 U.S.C. §1.56(c) most knowledgeable about the content of the information, the undersigned attorney of record

submits a translation of portions of an official action by a foreign examiner in which the references were cited. A copy of the official action is enclosed. The relevance to the pending U.S. patent application is that the references were cited in a foreign patent application corresponding to the above-captioned U.S. patent application. However, no independent analysis of the references, the accuracy of the statement of the foreign examiner or the claims of the foreign application under the laws of that country or the United States relative to the subject matter claimed in the present application has been made; the present understanding of the contents thereof by the undersigned being based on the translation of the foreign examiner's comments submitted herewith.

The Examiner is respectfully requested to initial the space adjacent to each document on the PTO-1449 form and return a copy of the PTO-1449 form to confirm that these documents have been considered by the Examiner and made of record in this application.

Although we believe that we have appropriately provided for any fees due in connection with this submission, the Commissioner is authorized to credit any overpayment or charge any deficiencies to/from our **Deposit Account No. 031721**. Two originally-executed copies of this form are being submitted.

Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at (617) 248-4038.

Respectfully submitted,

CHOATE, HALL & STEWART

June 24, 2003
Date

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1. In the description of the claims, even though Claims 5 through 12 of the present application must end* in the phrase "standard cell placement and a routing method," these claims simply read "method characterized" in the present application. Accordingly, the claims to be protected are unclear.

2. The inventions of Claims 1 and 2 of the present application relate to a standard cell, [the invention of] Claim 3 relates to a standard cell array, [the invention of] Claim 4 relates to a standard cell placement and a routing processing system, and [the inventions of] Claims 5 through 9 relate to a standard cell placement and a routing method. Therefore, the gist of these inventions relates to a standard cell placement and routing for a standard cell type of large-scale integrated circuit design.

However, [the inventions of] Claims 1 through 3 of the present application could easily be invented on the basis of the following inventions:

[1]† from Japanese Patent Application Kokai No. H5-304210 (Kokai disclosure date: November 16, 1993; Cited Invention 1), a standard cell structure which is a structure having diffusion layers and a TR forming polysilicon layer in an automatic layout cell using a standard cell system, which has at least two terminals for the same signal in a standard cell with a fixed height in order to allow routing from above and below, and which has means for distinguishing between data for forming internal elements in the part that has the same potential as the terminals and routing data from the data to the terminals;

[2] from Japanese Patent Application Kokai No. H10-144794 (Kokai disclosure date: May 29, 1998; Cited Invention 2), a semiconductor integrated circuit structure which makes it possible to improve the degree of freedom in design and the degree of integration in a standard cell that utilizes an existing placement and routing software by providing a plurality of global power supply nodes and a plurality of ground nodes in order to achieve a great increase in the current capacity of macrocells, further providing electric power supply node lines, and combining macrocells in the lateral direction; and

[3] from Japanese Patent Application Kokai No. H7-106649 (Kokai disclosure date: April 21, 1995; Cited Invention 3), a pattern layout method which allows the optimal pattern layout to be automatically arranged simply and rapidly in the following manner: specifically, a superconducting logic integrated circuit mounted on the board is divided into a plurality of sections, and a floor plan is divided into two regions according to the number of divisions of the integrated circuit, after which cells are arranged evenly in each of the divided sections, so that the power supply circuit, high-frequency electric power supply, and respective [sections of] the

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* Translator's note: Due to the syntactic difference between Japanese and English, this phrase would come at the beginning of each claim in English.

† Translator's note: [1] through [5] are added to clarify the cited inventions.

superconducting logic circuit are matched with each other by circuits that perform impedance matching.

[The inventions of] Claims 4 through 9 of the present application could easily be invented on the basis of the following inventions, [in addition to] a standard cell array structure of the type described in the above-mentioned cited inventions:

[4] from Japanese Patent Application Kokai No. H8-236634 (Kokai disclosure date: September 13, 1996; Cited Invention 4), a placement and routing method and a device for a semiconductor integrated circuit, comprising: an input device that inputs routing information, cell information, and design reference information; a placement and routing processing part based on fixed routing information and input information; a memory device; and an output device; and

[5] from Japanese Patent Application Kokai No. H7-94586 (Kokai disclosure date: April 7, 1995; Cited Invention 5), an optimal standard cell selection method which can minimize the effect of the layout results on the cell position and routing in delay optimization by means of a logic synthesis tool utilizing routing delay information following the automatic placement and routing.

End.

[Attachments]

Attachment 1. Japanese Patent Application Kokai No. H5-304210 (11/16/93): one copy
Attachment 2. Japanese Patent Application Kokai No. H10-144794 (5/29/98): one copy
Attachment 3. Japanese Patent Application Kokai No. H7-106649 (4/21/95): one copy
Attachment 4. Japanese Patent Application Kokai No. H8-236634 (9/13/96): one copy
Attachment 5. Japanese Patent Application Kokai No. H7-94586 (4/7/95): one copy

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
KOM-02001	09/604,530

Applicant: Atsuko KOZAI

Filing Date: June 27, 2000 | Group Art Unit: 2768

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
	AL	5-304210	11-16-1993	JP				
	AM	10-144794	5-29-1998	JP				
	AN	7-106649	4-21-1995	JP				
	AO	8-236634	9-13-1996	JP				
	AP	7-94586	4-7-1995	JP				

OTHER DOCUMENTS

(Include Author, Title, Date, Pertinent Pages, Etc.)

	AQ	
	AR	
	AS	

EXAMINER | DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.